

SDR Technology: Present Realities vs Future Possibilities



Manuel Uhm

Vice President, Marketing – Coherent Logix

Chief Marketing Officer, Board of Directors - Wireless Innovation Forum

2014-03-12

Coherent Logix Profile

Maker of low-power, high performance, C-programmable processors (HyperX™) and RF chipsets (rfX™) for the embedded systems market
– enabling low-power, real-time software defined systems.



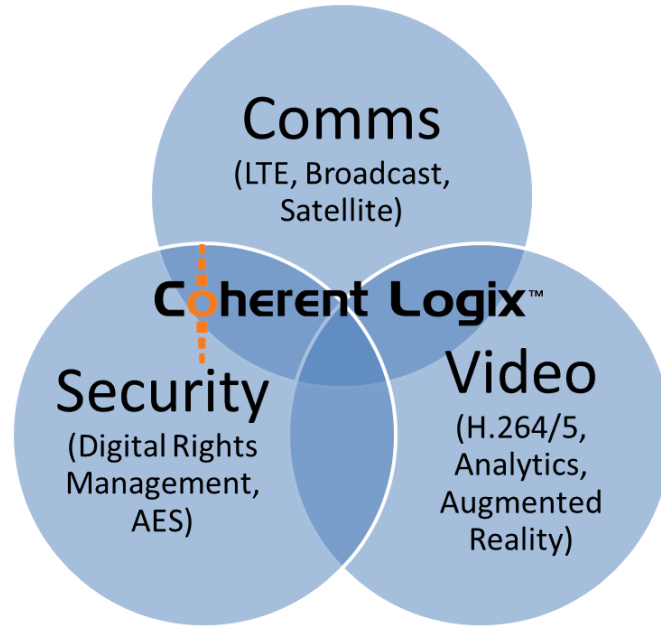
Wireless
Image / Video

Mil / Aero

High-Rel



The Coherent Logix Purpose



Coherent Logix is enabling the convergence of voice, video and image processing being securely transmitted wirelessly at very low power.

The world is changing too fast for traditional ASIC or even FPGA development cycles. Software Defined Systems are required since one can no longer anticipate every possible feature or requirement in advance, necessitating maximum flexibility at the lowest possible power consumption.

Introducing...the ***HYPERX***TM processor

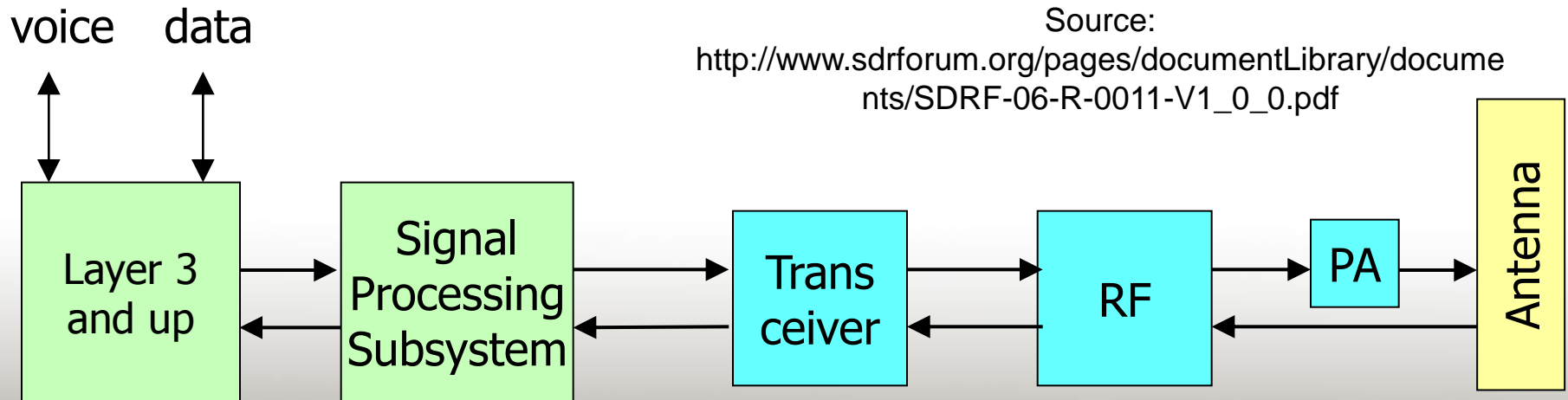
A very high performance, ultra-low power multicore (100) processor that:

- has **comparable power efficiency to an ASIC** - better than DSPs and FPGAs, and much better than GPPs and GPUs,
- has the **processing performance of an FPGA** to do tasks that normally require hardware accelerators completely in software, such as LTE turbo decoding and H.264 CABAC,
- has the **ease-of-use and C programmability of a GPP**, resulting in faster time-to-market
- may be **software upgraded** after deployment to support new air interfaces, codecs, advanced algorithms, or niche variants (i.e., LTE MBMS for broadcast or 4:2:2 chroma format) which other processors are not capable of supporting today,
- can **scale** from both a hardware (i.e., I/O) and software perspective (i.e., code reuse),
- is **low latency** and 100% deterministic,
- is **highly secure** with advanced digital rights management and security features.

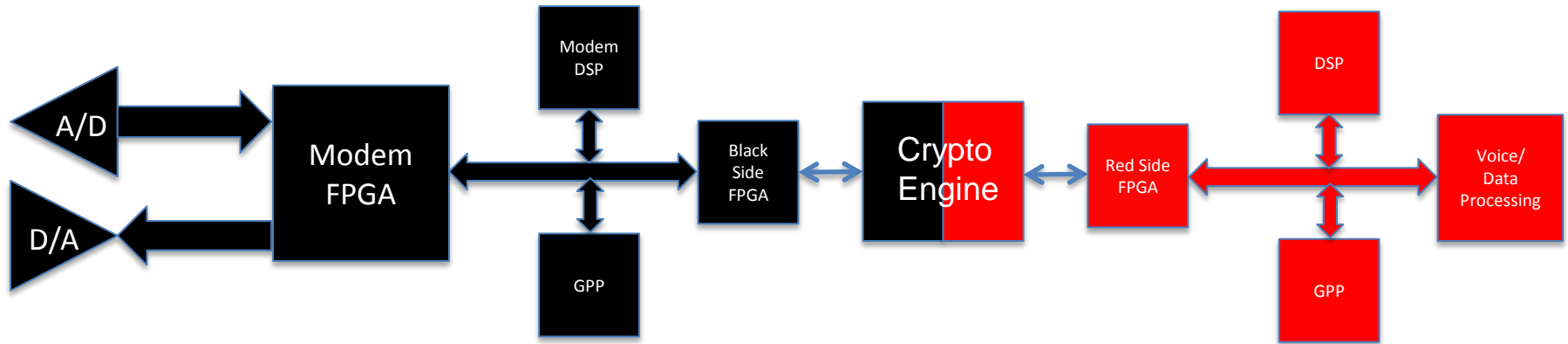
What is *Software Defined Radio* (SDR)?

According to the latest definition agreed upon between the IEEE P1900.1 and the Wireless Innovation Forum, an SDR is:

Radio in which some or all of the Physical Layer Functions are software-defined



Tactical Radios and Public Safety Radios are SDRs



Proven architecture, but:

- Extremely lengthy software development cycle
- No heterogeneous tools available to program, test or debug at system level, so test and verification is extremely difficult and tedious
- Very limited code portability – even moving VHDL to a next generation FPGA family is non-trivial

Cognitive Radios are SDRs

xG Technology: Coherent Logix HyperX-Based

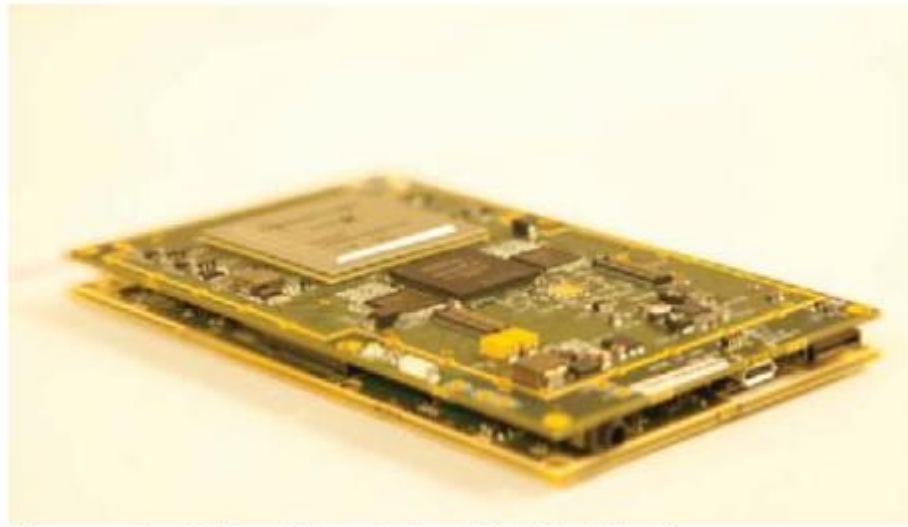
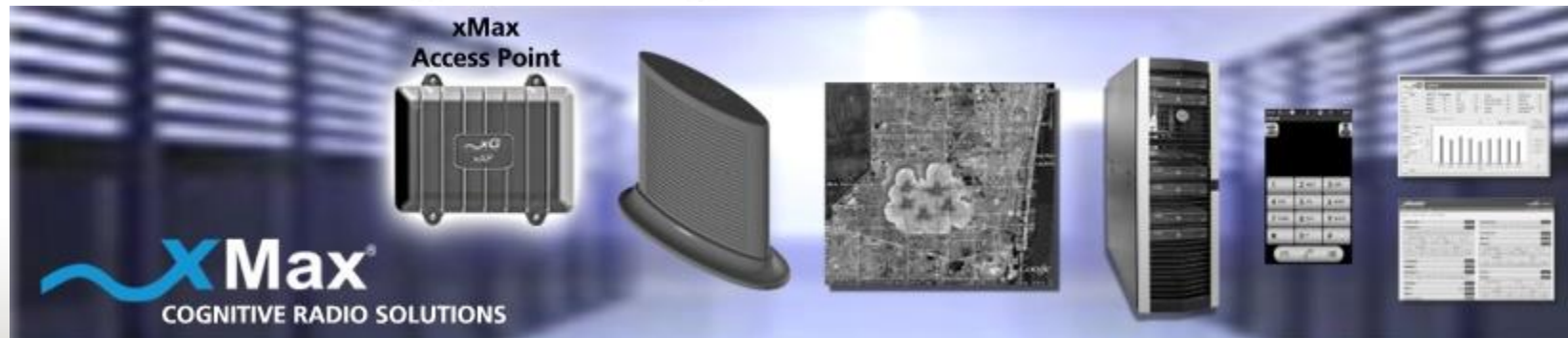


Figure 2. xMax Cognitive Radio Platform



Adaptrum: FPGA-Based



Carlson Wireless: FPGA-Based



This drove Carlson to a core design that is highly customizable. Running on a Xilinx Spartan-6 FPGA with an ARC CPU core and DSP blocks, Carlson is able to meet these requirements and provide TVWS service where needed, today. It's a relatively low cost implementation, able to hit

LTE Small Cells are SDRs

TI Small Cell Multi-Mode Architecture

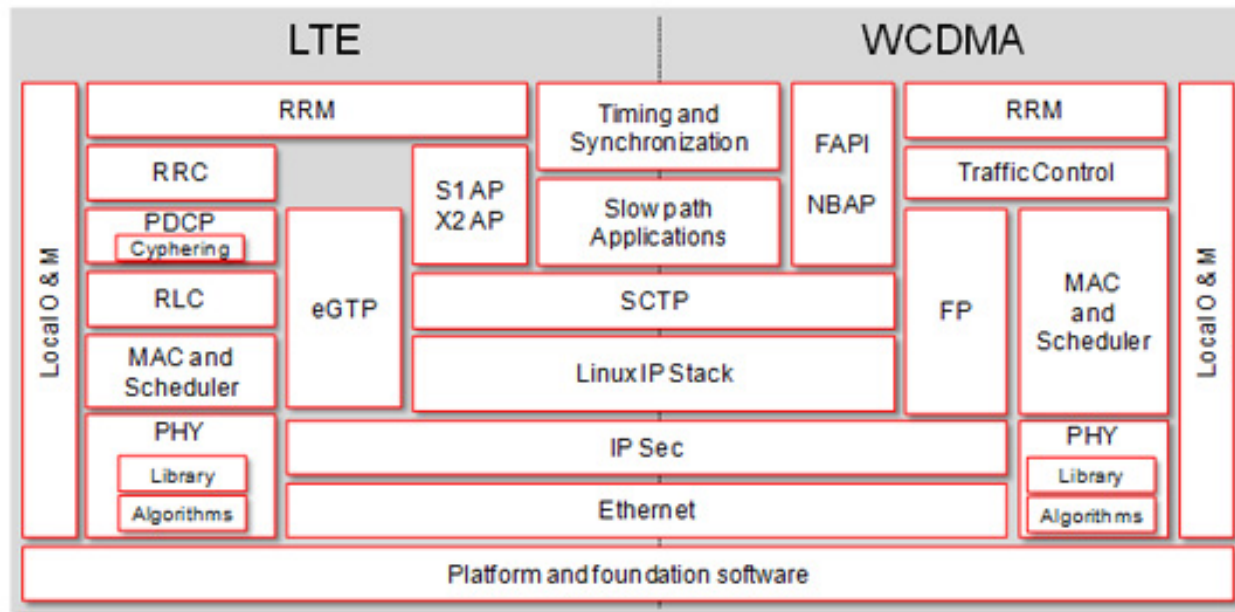
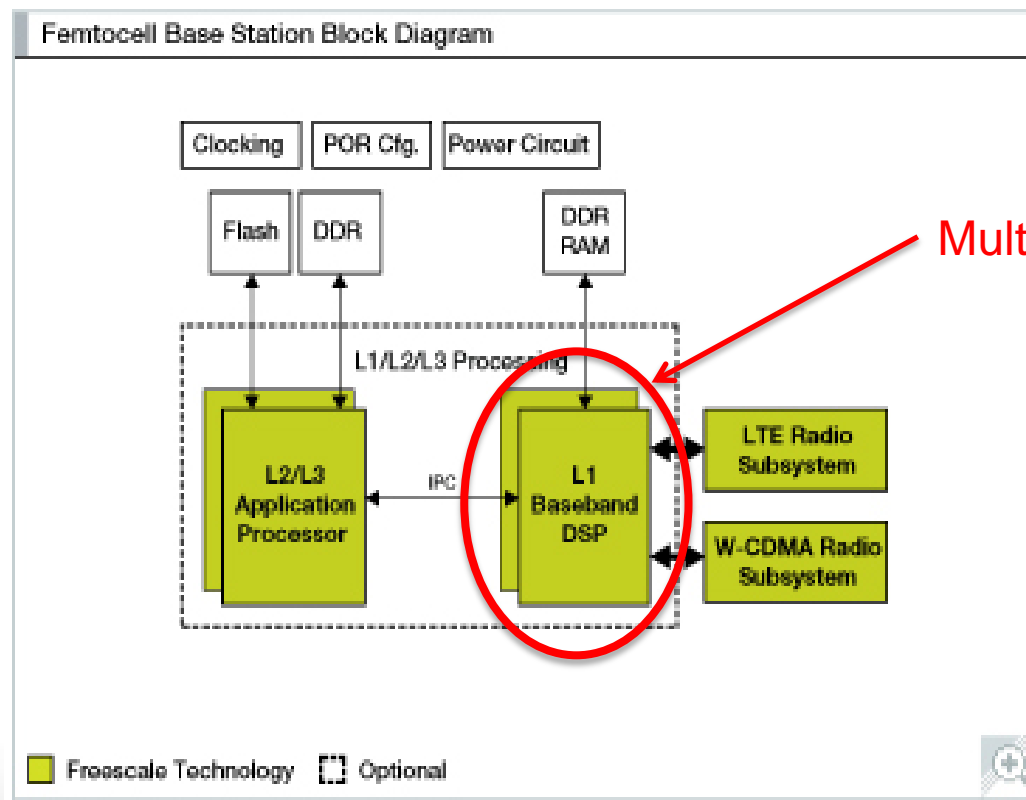


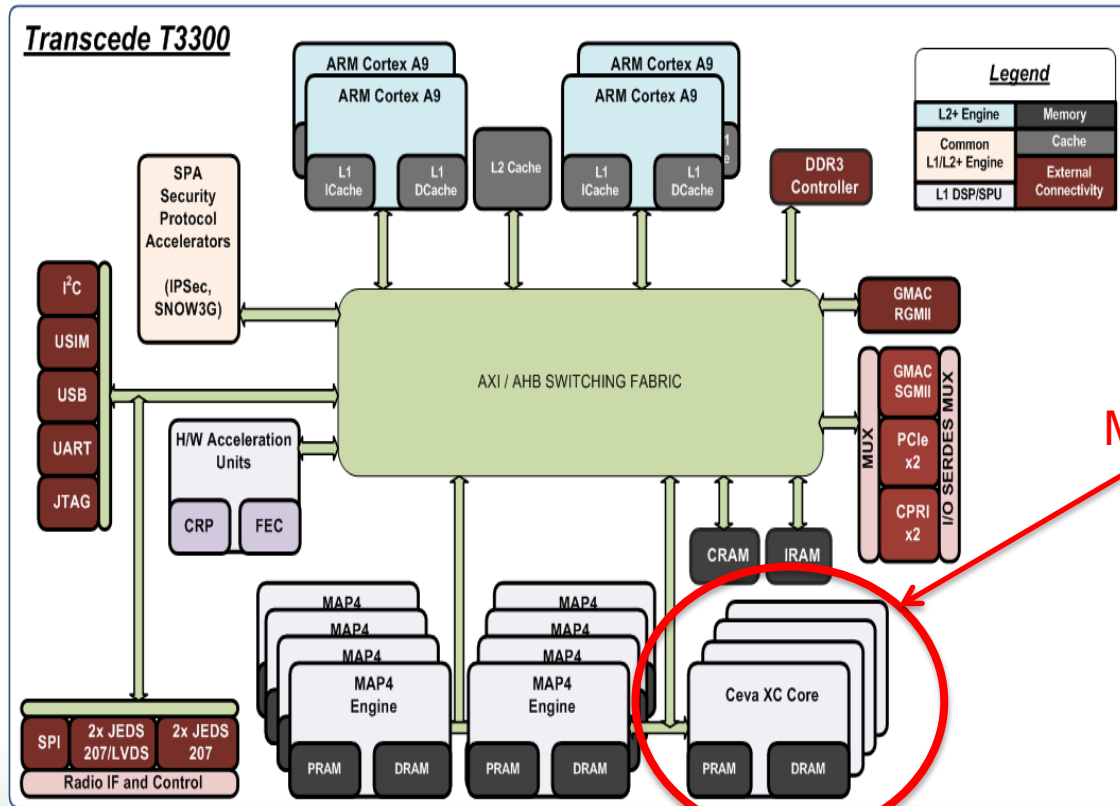
Figure 2: TI's small cell software architecture for LTE and WCDMA

Freescal Small Cell Chip

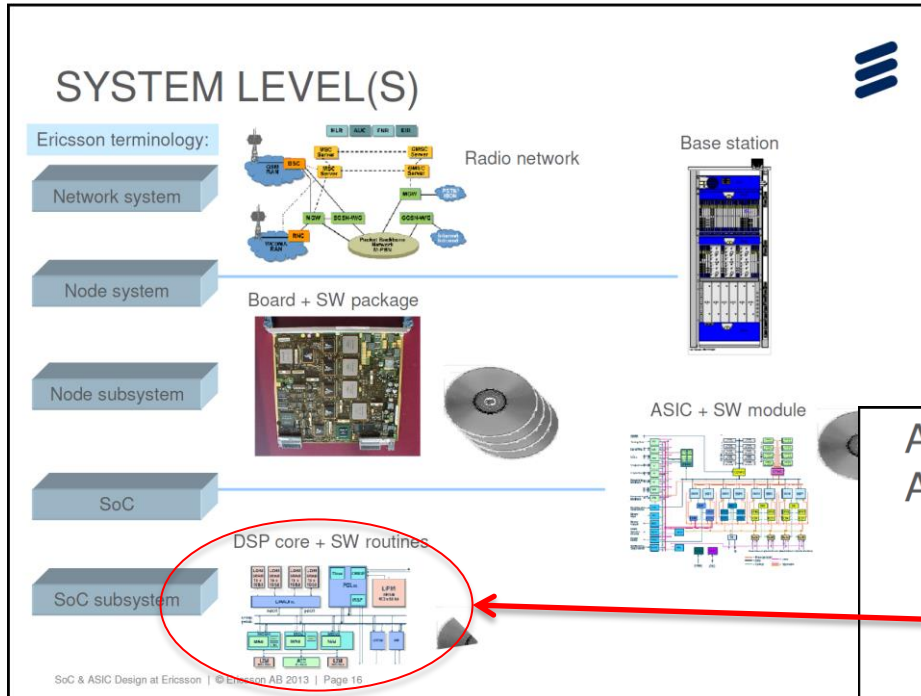


Multicore DSP Array

Intel/Mindspeed Small Cell Chip

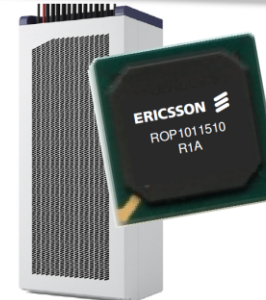


Macrocells are SDRs



AN LTE (4G) SIGNAL PROCESSING ASIC

RBS 6201

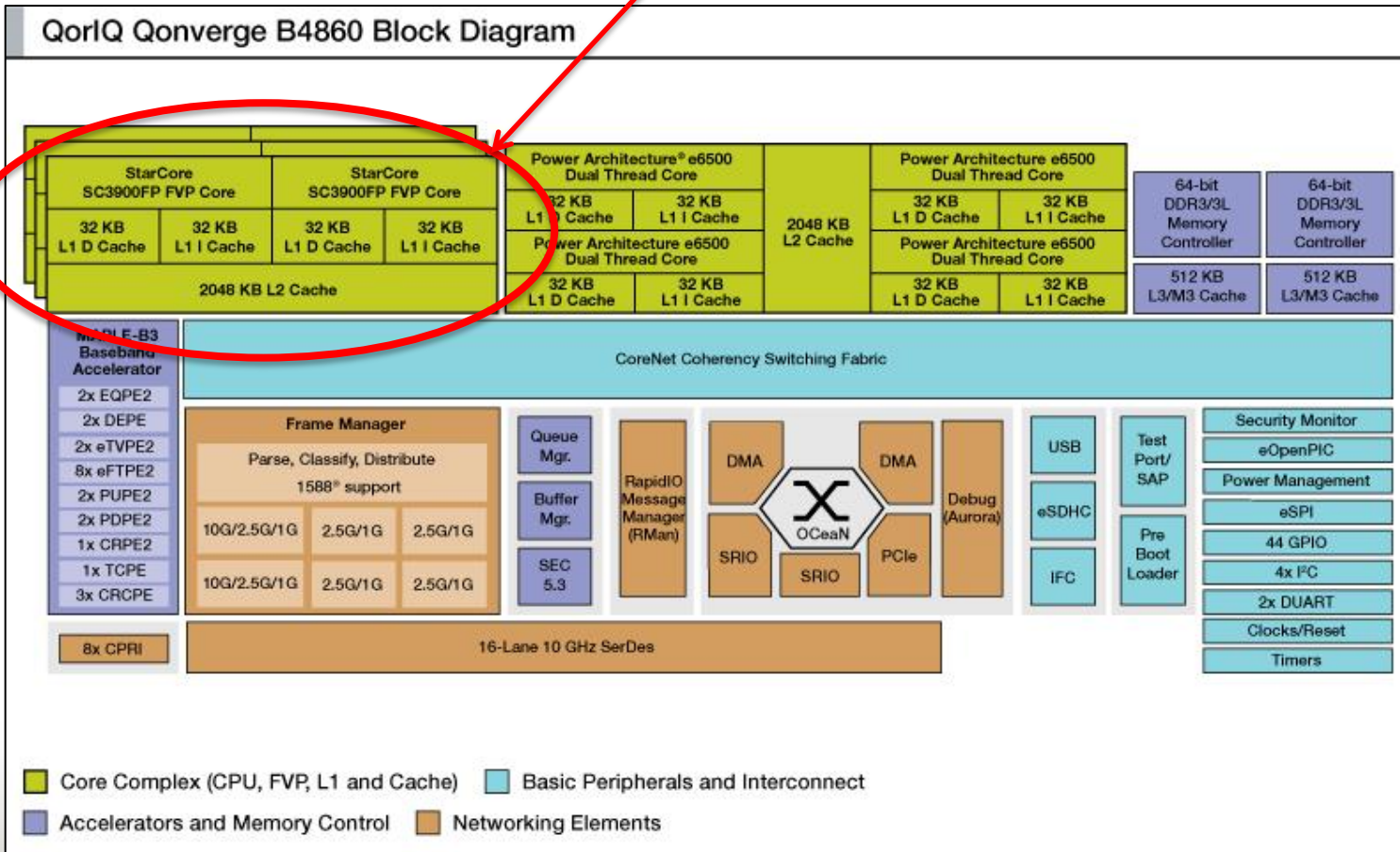


- › Uplink signal processing
- › 36 DSP cores
- › 1 CPU core
- › 29 M gates logic
- › 65 Mbit SRAM
- › 520 M transistors
- › 12 W power dissipation
- › 65 nm CMOS std cell
- › 675 ball flip chip PBGA package

SoC & ASIC Design at Ericsson | © Ericsson AB 2013 | Page 7

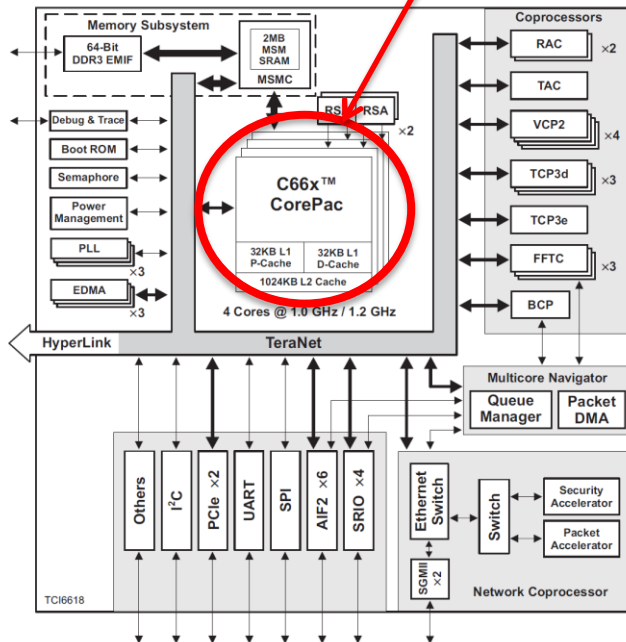
Freescape Large Cell Infrastructure Chip

Multicore DSP Array

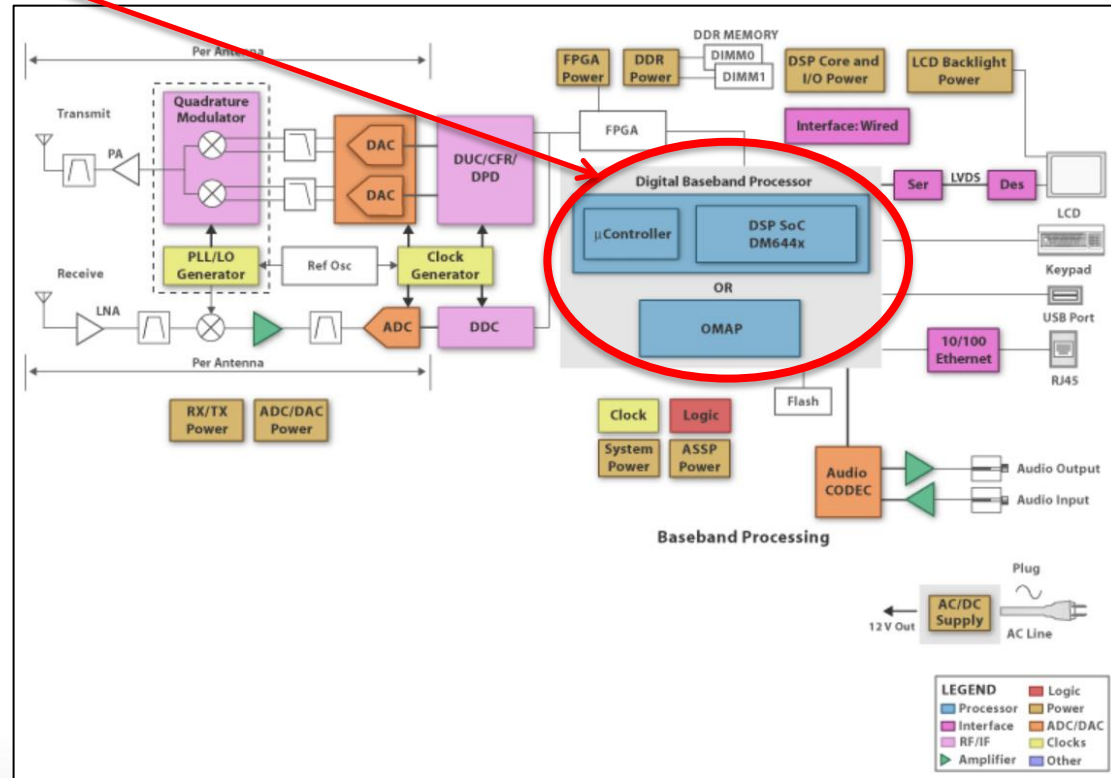


TI Large Cell Infrastructure Chip

Multicore DSP



TI Keystone basestation chipset

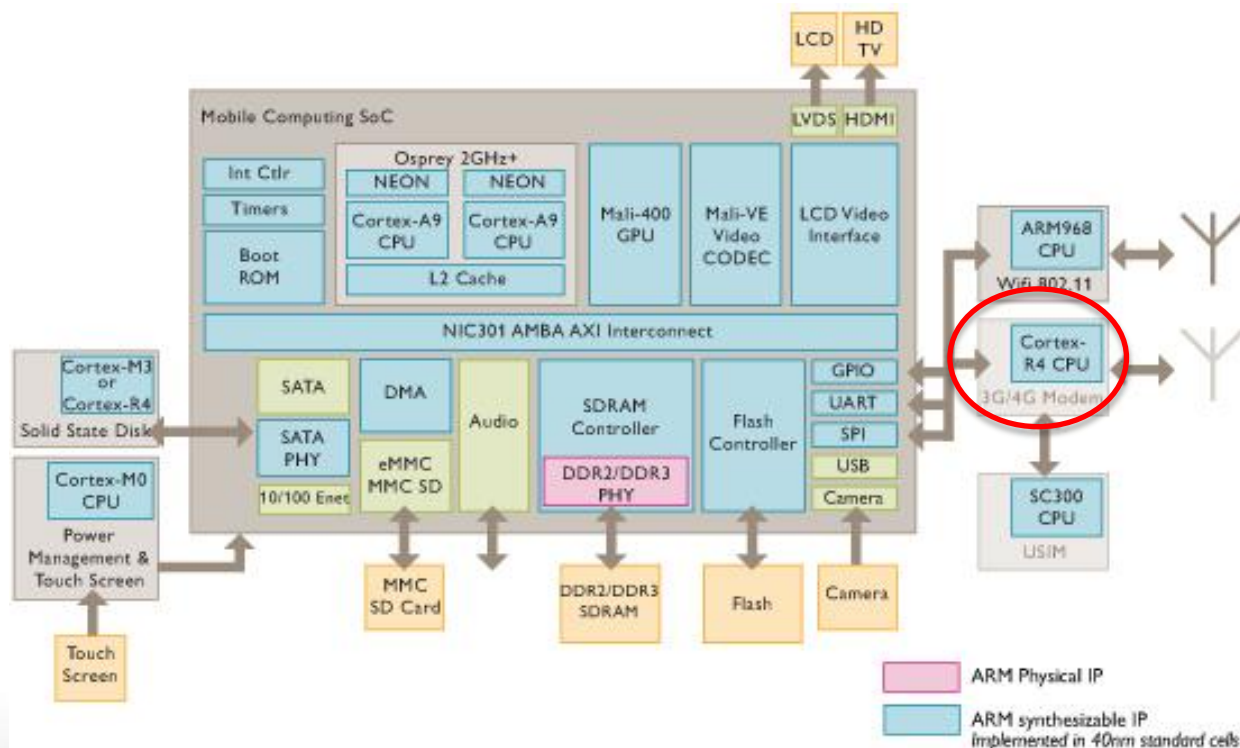


TI SDR System Architecture

Source: <http://www.ti.com/solution/software-defined-radio-sdr-diagram#>

Even Handsets are SDRs

ARM Mobile Device Reference Design



Qualcomm Snapdragon

- Snapdragon is the most successful handset chipset in the market today.
- Multiple Hexagon DSP cores are used to power the multimode SDR modem inside Snapdragon.
- Multiple generations (V1-V5) of Hexagon cores have been incorporated into Snapdragon for many years.
- It is in products from Apple, Samsung, Sony, LG, Nokia, Motorola, HTC, etc.

Key characteristics of modem & multimedia applications

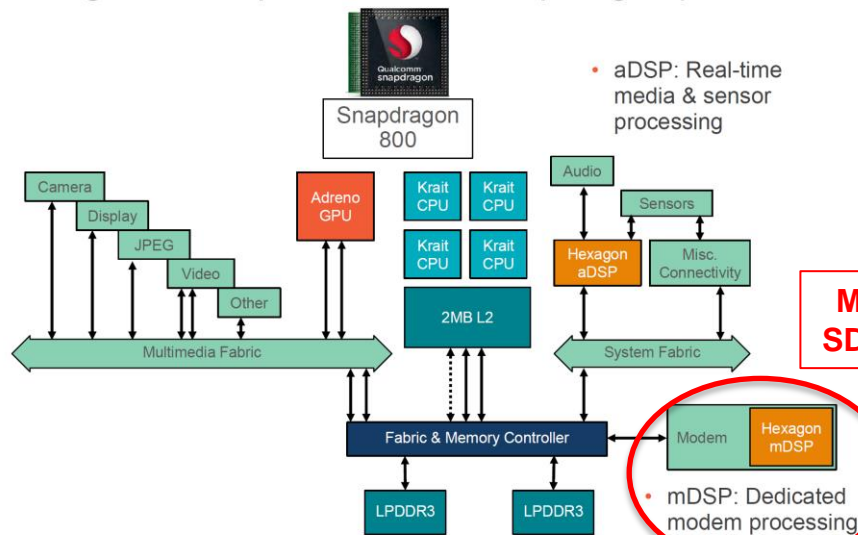
Requirements

- Require fixed real-time performance level (fps, Mbit/sec, etc.)
- Extremely aggressive power & area targets

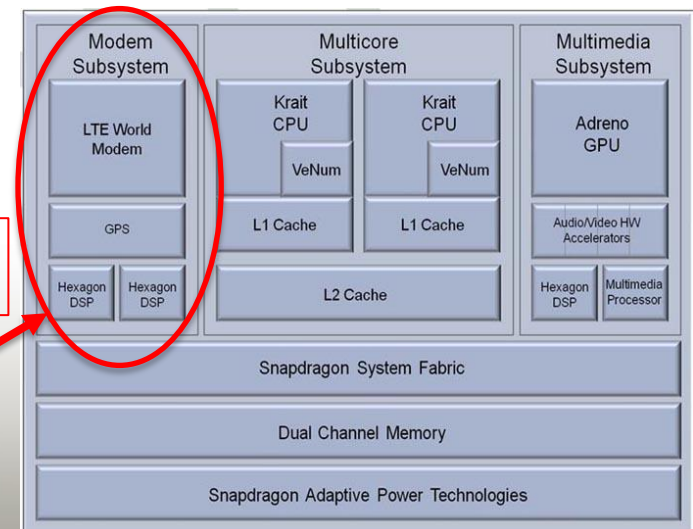
Characteristics

- Mix of signal processing & control code
 - For modem, Qualcomm does not use a split CPU/DSP architecture. All processing is done on Hexagon DSP
 - Multimedia apps have significant control in the RTOS & frameworks
- Heavy L2\$ misses
 - Multimedia is data intensive
 - Modem is code intensive

Hexagon™ DSP processors in Snapdragon products



Multimode SDR Modem



Qualcomm Technologies, Inc. All Rights Reserved

Qualcomm Technologies, Inc. All Rights Reserved

Nvidia and Icera

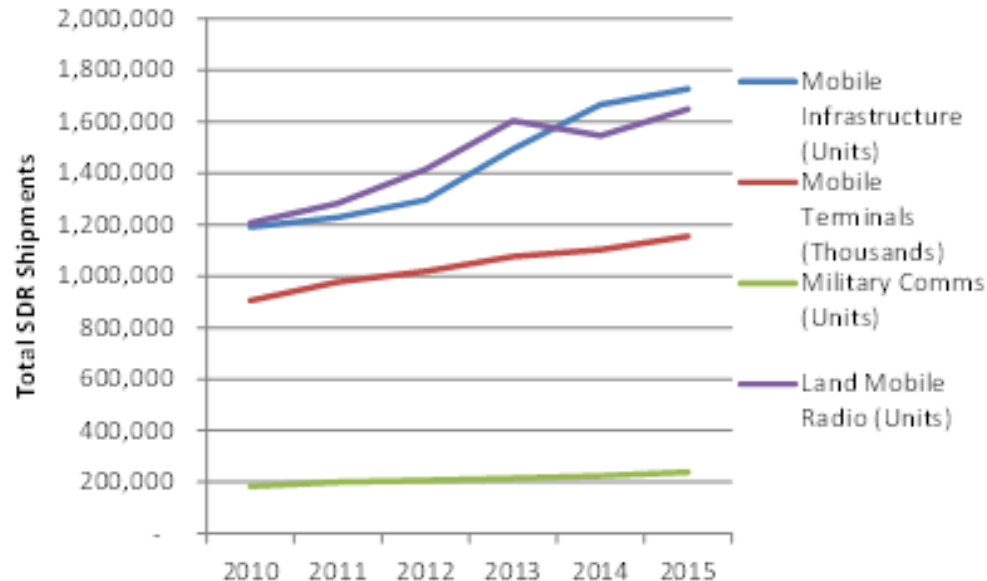


NVIDIA Tegra 4i

Highest Performing Single Chip Smartphone Processor
2.3GHz Quad CPU + 60 Core GPU + SDR LTE
Half the size of competing chip
Tegra 4 super phone experience

4G: The Success of SDR

SDR: Global Shipments



- Mobile Terminals represents the biggest segment by far
- SDR is taking analog market share in Public Safety and Private Mobile Radio (together known as Land Mobile Radio)
- Military Tactical SDR is growing more incrementally



Source: Wireless Innovation Forum SDR Market Size Study, 2011

Most 4G eNodeBs and UEs are based on SDR technology!

Why Has SDR Been So Successful for 4G?

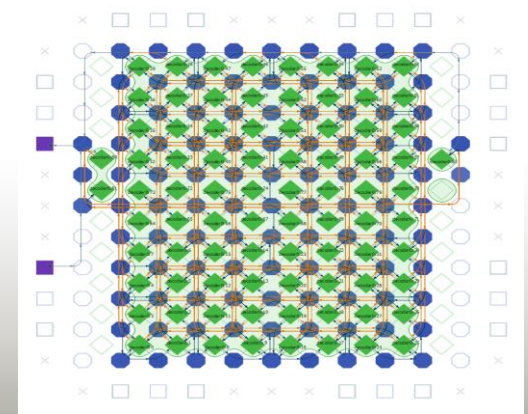
- Requirement for multi-mode support
- Flexibility to add features or adapt to ever evolving air interface protocols even after deployment, and do so in a manner that is CAPEX and OPEX friendly
- Development cost savings of code preservation
- Time-to-market benefit from software code reuse

Partial vs Fully Software Defined

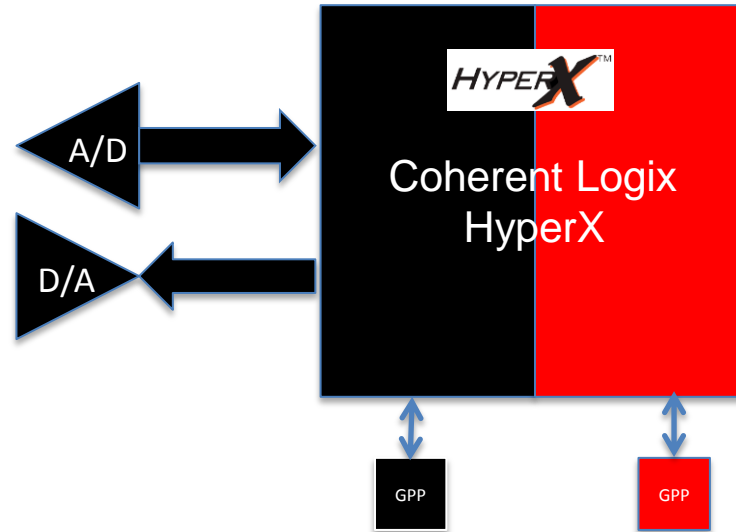
Some of the implementations previously shown are partially software defined since some key compute intensive functions are hardened (hardware accelerators), such as turbo decoding, MIMO and FFTs. This is done in order to achieve power and/or cost targets.

The downside is a loss of flexibility, for example, an inability to support an air interface with a different FEC scheme, or unable to improve radio performance by updating MIMO or demod algorithms.

At the 28nm node, it may finally be possible to achieve fully software defined implementations that can meet the power and cost targets.



Ideal Tactical Radio Modem Architecture



Single Chip Black Side/Red Side Modem:

- Ideal SWAP (Size, Weight And Power) solution
- Major reduction in software development cycle
 - “5x productivity improvement...as compared to FPGA...”
- No VHDL required at all – all code in ANSI C
- Can program, test and debug at system level, reducing the time for test and validation
- Significant increase in code portability – all code in ANSI C

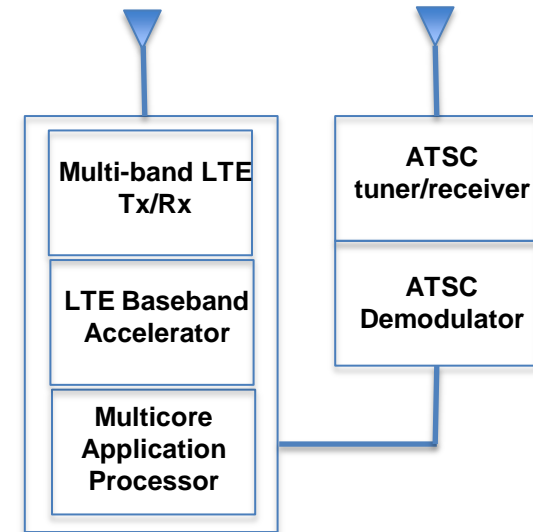
Next Generation SDR Chipset for ATSC 3.0 Consumer Devices

Today's radio chipset

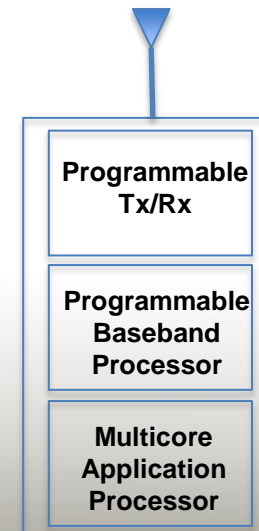
- External ATSC tuner/receiver
 - Added BOM cost, royalty, circuit board real estate, and power consumption
- LTE RF support is limited to a few bands (out of 40+ 3GPP LTE bands)
- Baseband processing is mostly hardwired circuitry with limited flexibility
- Broadcast and broadband are separate functions

New generation radio chipset

- Programmable baseband processor to support all waveforms
 - For example, ATSC and LTE at the same time
 - Single chip solution, no separate ATSC chipset
- Programmable RF to support all bands from VHF/UHF to a min. of 5GHz
- Cost/size/power neutral when compared to today's chipset
 - No compromise while supporting more functionalities
- SW stack to support broadcast/broadband convergence and off-load



Current Chipset



New Generation Chipset

Next Generation Handset by Top-5 OEM

Working with one of the world's largest handset manufacturers to define and design a multi-purpose chip and software-reprogrammable system, for next generation handset.

The chip must support different types of modems, as well as camera, computational imaging, navigation, augmented reality, sensor processing, and other future signal-processing requirements.

Since it is difficult to define the ASIC requirements 18 to 24 months ahead, a Software-defined flexible chip is required.

This will be a next generation HyperX processor at 20/28nm.

HyperX Processor Figures of Merit

	hx3100	hx4XXX	2016 (hx4XXX)	2016 (hx5XXX)
Process technology	65nm	28 nm	16 nm	16 nm
GFLOPS/W (Based on FIR)	12	113	191	470
GOPS/W (based on FIR)	46	905	1531	3764
GOPS/W (based on Turbo decoder and ME)	77	1358	2296	5647
Power consumption (mW; LTE UE baseband)	3300	250	168	86
Power consumption (mW; H.264/AVC HP 1080p30 L4 : Prof. Qual.)	4500	274	184	94

Conclusions

- **SDR is the de facto standard for almost all radios today**
- **Key factors that drove adoption are flexibility, development cost savings and faster time-to-market**
- **But some SDRs today are only partially software-defined**
- **The future trend favors completely software-defined implementations**
 - No hardware accelerators, no RTL, no VHDL!
- **Multi-core processors, such as the HyperX processor, are an enabling technology for complete SDR implementations**

Thank you!

Manuel Uhm
Vice President, Marketing
manuel@coherentlogix.com
+1 (408) 600-1456